REMARKS

Claims 1-3, 5, 18-51, and 56-87 are currently pending, claims 4, 6-17, 52-55, have been canceled, and claims 18-51 and 56-66 are withdrawn. Claims 71-86 are new. No new matter has been included. Applicants reserve the right to pursue original and other claims in this and in other applications.

Claim 1 stands rejected under 35 U.S.C. §112, first paragraph as allegedly failing to comply with the written description requirement. Applicants respectfully disagreed. However, to advance the prosecution of this application and for clarity, claim 1 has been amended. Thus, the rejection of claim 1 should be withdrawn.

Applicants appreciate the Examiner's time and attention during a telephonic conference on April 4, 2007 with Applicants' representative. During the conference, Examiner Giles identified the elements of Kole (U.S. Pat. No. 6,501,064)("Kole") that allegedly correspond to elements of the claimed invention. Examiner Giles indicated that:

- Kole's element 71 (FIG. 4B) corresponds to first and second voltages of claim 1.
- Kole's element 30 (FIG. 4B) corresponds to element 186 (FIG. 7) of the claimed invention.
- Kole's intersection of lines between elements 20, 30, and S1 (FIG. 4B) corresponds to element A (FIG. 7) of the claimed invention.
- in Kole, an inactive signal corresponds to a Ground voltage or Ground potential.

Claims 1-4, 6-16, 52-55, and 67-70 stand rejected under 35 U.S.C. 103 (a) as being anticipated by Kole (U.S. Pat. No. 6,501,064)("Kole") in view of Kokubun et al. (U.S. Pat. Pub. No. 2003/0146993) ("Kokubun") in further view of Merrill (U.S. Pat. Pub. No. 2002/0036700) ("Merrill"). Applicants respectfully traverse this rejection.

Claim 1 recites:

an image array pixel comprising:

a charge storing node;

a photosensor coupled to said charge storing node;

a controllable voltage source for supplying one of a first and second voltage level, said first voltage level being higher than said second voltage level;

a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being coupled to an output of said controllable voltage source, the other of said source/drain regions being coupled to said charge storing node;

a reset control circuit coupled to a gate of said reset transistor, said reset control circuit for selectively providing a first reset control signal at a first level and a second reset control signal at a second level, said first level being higher than said second level,

said reset control circuit and controllable voltage source being controllable during first, second, and third time intervals such that:

during said second time interval, said reset transistor control circuit supplies said second reset control signal to said gate of said reset transistor while said controllable voltage source provides said second voltage to partially remove charges from said photosensor,

during said third time interval, said reset transistor control supplies said first reset control signal to said gate of said reset transistor, said controllable voltage source provides said first voltage to substantially remove all charges from said photosensor.

Kole discloses:

An image pick-up [that] includes a number of active sensor elements ...arranged in an array and a number of conductive lines extending over the surface of the array for the transfer of supply and signals. Each sensor element includes a light sensor (20) and an amplifier. According to the invention, a reduction in the number of lines can be achieved while functionality is maintained. In a first and a second embodiment (11; 12), a sensor element includes a first switch (S1)

> associated with the sensor and a second switch (S2; S3) associated with the amplifier, the switches being controlled by a common control signal. In a third embodiment (13), a sensor element includes a series arrangement of a first switch (S1) and a second switch (S2) included between the sensor and a supply line. In a fourth embodiment (14), a select signal is also used as a supply for the amplifier.

(Kole, Abstract)

Kole fails to disclose or suggest said "said reset control circuit and controllable voltage source being controllable during first, second, and third time intervals such that: during said second time interval, said reset transistor control circuit supplies said second reset control signal to said gate of said reset transistor while said controllable voltage source provides said second voltage to operate said reset transistor to partially remove charges from said photosensor, during said third time interval, said reset transistor control supplies said first reset control signal to said gate of said reset transistor, said controllable voltage source provides said first voltage to substantially remove all charges from said photosensor." As such, the rejection of claim 1 should be withdrawn and the claim and its dependant claims allowed.

Kokobun is cited by the Office as providing two different voltage sources for providing first and second voltages. Office Action, page 3.

Kokobun fails to disclose a "controllable voltage source for supplying one of a first and second voltage level, said first voltage level being higher than said second voltage level". To the contrary, Kokobun only discloses a voltage source providing a single voltage. See for example, Kokobun's FIG. 4 reproduced below, which shows only one voltage VR. Thus, Kokobun does not disclose "a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being coupled to an output of said controllable voltage source, the other of said source/drain regions being coupled to said charge storing node."

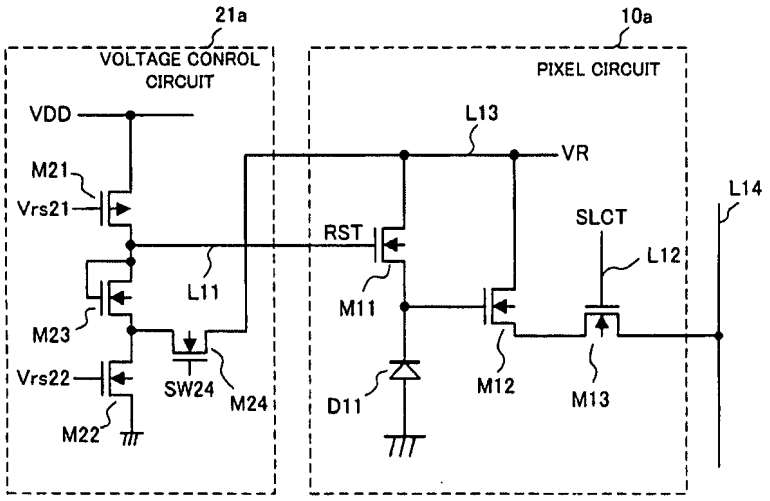

FIG. 4

Kokubun also fails to cure the deficiency of Kole and fails to disclose or suggest "said reset control circuit and controllable voltage source being controllable during first, second, and third time intervals such that: during said second time interval, said reset transistor control circuit supplies said second reset control signal to said gate of said reset transistor while said controllable voltage source provides said second voltage to operate said reset transistor to partially remove charges from said photosensor, during said third time interval, said reset transistor control supplies said first reset control signal to said gate of said reset transistor, said controllable voltage source provides said first voltage to substantially remove all charges from said photosensor." As such, the rejection of claim 1 should be withdrawn and the claim and its dependant claims 2-7 allowed over the combination of Kole and Kokubun.

Merrill is cited by the Office for the proposition that "a row select transistor being switchably coupled to the first and second voltage and the reset transistor and row select transistor having their own control lines."

Merrill fails to cure the deficiency of Kole and Kokubun and fails to disclose or suggest "a controllable voltage source for supplying one of a first and second voltage level, said first voltage

level being higher than said second voltage level". Nor does Merrill disclose "a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being coupled to an output of said controllable voltage source, the other of said source/drain regions being coupled to said charge storing node."

Merrill also fails to cure the deficiency of Kole and Kokubun and fails to disclose or suggest "said reset control circuit and controllable voltage source being controllable during first, second, and third time intervals such that: during said second time interval, said reset transistor control circuit supplies said second reset control signal to said gate of said reset transistor while said controllable voltage source provides said second voltage to operate said reset transistor to partially remove charges from said photosensor, during said third time interval, said reset transistor control supplies said first reset control signal to said gate of said reset transistor, said controllable voltage source provides said first voltage to substantially remove all charges from said photosensor." As such, the rejection of claim 1 should be withdrawn and the claim and its dependant claims 2-7 allowed over the combination of Kole and Kokubun and Merrill.

With respect to claim 67, the combination of Kole, Kokubun, or Merrill fail to disclose a "reset transistor having source/drain regions on opposite sides of a gate of said reset transistor, one of said source/drain regions being switchably coupled to a first and second voltage, the other of said source/drain regions being coupled to said node, the gate of said reset transistor being coupled to a reset control circuit" as noted above with respect to claim 1. As such, the rejection of claim 67 should be withdrawn and claim 67 and its dependant claims allowed over the combination of Kole, Kokubun and Merrill.

Claim 5 stands rejected under 35 U.S.C. 103 (a) as being anticipated by Kole in view of Kokubun in further view of Mizuno (U.S. Pat. Pub. No. 5,912,463) (Mizuno). Applicants respectfully traverse this rejection.

Claim 5 is dependent from claim 1 and is allowable over the combination of Kole and Kokubun for at least the reasons noted above.

Claim 5 adds the limitation that "wherein said pixel does not receive any light."

Mizuno is cited by the Office for the proposition that the pixel does not receive any light. However, Kole discusses its photodiodes receiving light, which is contrary to the suggestion of the Office that Kole is "silent" regarding this feature. See, at least, Kole, Col. 2, lines 17-45, "...a photo sensitive element which provides at its output 22 an electric signal which corresponds to the light L received by the light sensor..." Thus, Mizuno teaches away from attempting to combine Kole with the teachings of Mizuno. Thus, the rejection of claim 5 should be withdrawn and the claims allowed over the combination of Kole, Kokubun, and Mizuno.

With respect to new claim 71, the combination of Kole, Kokubun and Mizuno fail to disclose "a controllable voltage source for selectively supplying one of a first lower voltage level and a second higher voltage level to a voltage supply line." Further, the combination of Kole, Kokubun and Mizuno fail to disclose "during a first time period, said reset transistor is supplied with a gate control signal at a first level while said controllable voltage source supplies said second voltage level to said voltage supply line, during a second time period, said reset transistor is supplied with a gate control signal at a second level lower than said first level but above a threshold voltage of said reset transistor while said controllable voltage source supplies said second voltage level to said voltage supply line." As such, claim 72 and its dependant claims are allowable over the combination of Kole, Kokubun and Mizuno.

New claim 75 recites:

a pixel array comprising:

at least one pixel circuit comprising:

a storage node for storing charges;

a reset transistor for controlling the charges stored at said storage node;

a circuit for operating said reset transistor to fill the storage node with electrons, to partially remove electrons from said storage node, and to substantially remove all charges from said storage node; and

a readout circuit for providing a first signal representing charges at said storage node after electrons are partially removed from said storage node and a second signal representing charges at said storage node after all charges are removed from said storage node.

With respect to new claim 75, the combination of Kole, Kokubun, and Mizuno fail to disclose "a readout circuit for providing a first signal representing charges at said storage node after electrons are partially removed from said storage node and a second signal representing charges at said storage node after all charges are removed from said storage node." As such, claim 75 is allowable over the combination of Kole, Kokubun, and Mizuno.

New claim 80 recites:

A pixel comprising:

a first voltage source having an output switchable between a first and second reset supply voltage in response to a first control signal;

a charge storage region;

a reset transistor connected between said first voltage source and said charge storage region; and

a control circuit for providing a gate control voltage to a gate of said reset transistor, said control circuit selectively providing a first operating control voltage and a second operating control voltage to said reset transistor, said second operating control voltage being less than said first operating control voltage.

Kole, Kokubun, and Mizuno fail to disclose "a first voltage source having an output switchable between a first and second reset supply voltage... [coupled] to said charge storage region" and "a control circuit for ...providing a first operating control voltage and a second operating control voltage to said reset transistor...." As noted above with respect to claim 1. As such, claim 80 is allowable over the combination of Kole, Kokubun, and Mizuno.

With respect to new claim 84, the combination of Kole, Kokubun, and Mizuno fail to disclose a "control circuit for operating said reset transistor and said sample and hold circuit for providing a correlated double sampling and holding of a charge integrated signal and a full reset signal during a one sample and hold period and for providing a sampling and holding of a first full reset signal with said reset transistor receiving a first gate control signal and a second less than full rest signal with said reset transistor receiving a second gate control signal which is lower than said first gate control signal during a second sample and hold period." As such, claim 84 is allowable over the combination of Kole, Kokubun, and Mizuno.

In view of the above, Applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

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